IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-4 (Cancelled):

Claim 5 (Currently Amended): A method of processing a semiconductor device according to claim [[1]]21, wherein said information on the exposure distortion caused by the first exposure tool and information on the exposure distortion caused by the second exposure tool used in said step of rendering the exposure of the second overlay measurement mark and second pattern by using the second exposure tool fitted up with the second mask are stored in a memory in advance.

Claim 6 (Currently Amended): A method for processing a semiconductor device according to claim [[1]]21 further including the step of displaying information on the overlay accuracy between the first circuit pattern and the second circuit pattern.

Claims 7-20 (Cancelled):

Claim 21 (New): A method of processing a semiconductor device comprising the steps of:

applying photo-resist to a surface of a substrate to be processed;

rendering exposure of first layer overlay marks and a first layer circuit pattern to the substrate coated with the photo-resist by using a first exposure tool which is fitted up with a first mask;

processing the substrate, which has been rendered with the exposure of the first layer overlay marks and the first layer circuit pattern, to form thereon first layer overlay marks and a first layer circuit pattern;

applying photo-resist to the surface of the substrate on which the first layer overlay marks and the first layer circuit pattern have been formed;

rendering exposure of second layer overlay marks and a second layer circuit pattern to the substrate coated with the photo-resist by using a second exposure tool which is fitted up with a second mask;

processing the substrate, which has been rendered with the exposure of the second layer overlay marks and the second layer circuit pattern, to form thereon second layer overlay marks and a second layer circuit pattern; and

wherein said step of rendering the exposure of the second layer overlay mark and the second layer circuit pattern by using the second exposure tool fitted up with the second mask includes, beforehand, the steps of calculating matching error in circuit pattern areas between exposure distortions of first-layer and second-layer circuit pattern areas being smaller than an exposure field, calculating matching error at overlay mark positions between exposure distortions of first-layer and second-layer overlay mark positions, calculating a modification value which relates both said matching errors, calculating a first exposure condition correction value based on an overlay measurement result which is a result of actual exposure by said second exposure tool by positioning with reference to overlay marks, and modifying said

calculated first exposure condition correction value with said modification value to obtain a second exposure condition correction value for rendering the exposure by using said second exposure tool.